In re Patent Application of
BEAUJOIN ET AL.
Serial No. **10/075,113**
Filed: **FEBRUARY 13, 2002**

REMARKS

Applicants thank the Examiner for the careful and thorough examination of the present application. Claims 9-31 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Drawings

In the Office Action, the Examiner requested a proposed drawing correction to illustrate "a simple flowchart with boxes containing the steps of the method" to "aid in the understanding of the claimed invention. However, Applicants point out that Fig. 1 of the present application illustrates the structural detail that is essential for a proper understanding of the disclosed invention as required by 37 CFR 1.83. Also, Fig. 2 is a timing diagram that is used to illustrate the method described on pages 5-10 of the present specification. Accordingly, Applicants maintain that the current drawings comply with the requirements of 37 CFR 1.83 and no other drawing correction is required.

II. Invention

As shown in FIGS. 1-4, for example, the disclosed invention is directed to a sequential access memory array test that allows a particularly simple implementation leading to an extremely small overall size of the test logic. The invention provides a method of testing a sequential access memory plane adapted to store p words each of n bits. In this method p test words each made up of n test bits are written in the memory array. The p test words are sequentially extracted from the memory plane and the test bits of the extracted words are compared with expected binary data bits

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III. The Claims are Patentable

Claims 9-31 were rejected in view of Kim et al. (US Patent No. 6,108,802) in view of Martens (US Patent No. 5,751,727) taken together or in combination with Zorian et al. (U.S. 6,330,696) and/or Biskup et al. (U.S. 6,751,757) for the reasons set forth on pages 2-8 of the Office Action. Applicants contend that Claims 9-31 clearly define over the cited references, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §103 is requested.

The independent claims include testing a sequential access memory plane by writing p test words each made up of n test bits in the memory array, and then extracting the p test words sequentially from the memory plane to compare with expected binary data bits. It is this combination of features which is not fairly taught or suggested in the cited references and which patentably defines over the cited references.

In the Kim et al. patent, a variety of FIFOs, including single and dual port, RAM-type and/or having a ring type addressing mechanism, are tested by causing the FIFOs to execute a test method having of a series of steps. Upon execution, the steps cause the FIFO to manifest a variety of faults. This test method manifests faults by monitoring the outcome of operations and the values of particular flags indicative of normal FIFO operation. As correctly recognized by the Examiner, the method does not include sequentially extracting p test words from the memory plane and comparing them with the expected binary data bits.

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The Martens et al. patent is directed to a dynamic scannable latch circuit for high-speed memory arrays utilized in high performance integrated circuit devices, wherein the high-speed memory arrays include data-bearing bitlines. The dynamic scannable latch circuit includes a group of scannable latch circuits for serially reading data from high-speed memory arrays during memory-testing cycles wherein each scannable latch circuit provides a scan output to a scan input of a second or next scannable latch circuit in a series of scannable latch circuits.

First, Applicants maintain that the Examiner has mischaracterized the Martens et al. reference. Marten et al. teaches that the array has the capability of reading data out serially in certain testing conditions. As such the memory elements are connected in series. However, nothing in Marten et al. discloses testing a sequential access memory plane by extracting p test words sequentially from the memory plane to compare with expected binary data bits, as claimed.

Furthermore, none of the other cited references, relied upon by the Examiner as teaching various features such as a checkerboard pattern and specific circuit implementation, makes up for the deficiencies of the Kim et al. and Marten et al. references as discussed above.

Additionally, Applicants maintain that the Examiner is impermissibly using the teachings of Applicants' own patent application as a roadmap to modify the prior art. For example, as noted above, both Kim et al. and Marten et al. teach the use of a memory test that does not include extracting p test words sequentially from the memory plane to compare with expected binary data bits. It is Applicants disclosure that teaches such a feature.

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As the Examiner is aware, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim features. The initial burden is on the Examiner to provide some suggestion of the desirability of doing what the Applicants have done. To support the conclusion that the claimed invention is directed to obvious subject matter, either the reference must expressly or impliedly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. Both the suggestion to make the claimed combination and the reasonable expectation of success must be founded in the prior art and not in Applicants' disclosure.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Furthermore, no proper modification of the teachings of the references could result in the invention as claimed. Accordingly, for at least the reasons given above, Applicants maintain that the cited references do not disclose or fairly suggests the invention as set forth in Claims 9, 11, 14, 20 and 26. Thus, the rejections under 35 U.S.C. §103(a) should be withdrawn.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their

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dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

IV. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone in order to resolve such informalities.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 9th day of December, 2004.

Dawn K. Kumler